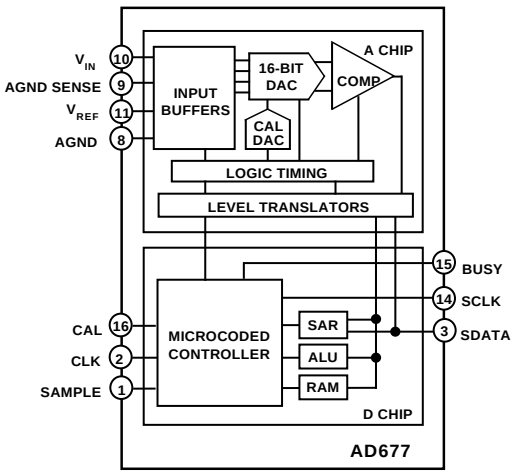
16-Bit 100 kSPS Sampling ADC

AD677

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Serial Output
16 Bits No Missing Codes
±1 LSB INL
–99 dB THD
92 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD677 is a multipurpose 16-bit serial output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD677 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD677 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD677 operates from +5 V and ±12 V supplies and typically consumes 450 mW using a 10 V reference (360 mW with 5 V reference) during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided to remotely sense the ground potential of the signal source. This can be useful if the signal has to be carried some distance to the A/D converter. Separate analog and digital grounds are also provided.

The AD677 is available in a 16-pin narrow plastic DIP, 16-pin narrow side-brazed ceramic package, or 28-lead SOIC. A parallel output version, the AD676, is available in a 28-pin ceramic or plastic DIP. All models operate over a commercial temperature range of 0°C to +70°C or an industrial range of –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Autocalibration provides excellent dc performance while eliminating the need for user adjustments or additional external circuitry.
2. ±5 V to ±10 V input range ($\pm V_{REF}$).
3. Available in 16-pin 0.3" skinny DIP or 28-lead SOIC.
4. Easy serial interface to standard ADI DSPs.
5. TTL compatible inputs/outputs.
6. Excellent ac performance: –99 dB THD, 92 dB S/(N+D) peak spurious –101 dB.
7. Industry leading dc performance: 1.0 LSB INL, ±1 LSB full scale and offset.

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AD677–SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
Total Harmonic Distortion (THD)[2]							
@ 83 kSPS, T_{MIN} to T_{MAX}		–97	–92		–99	–95	dB
@ 100 kSPS, +25°C		–97	–92		–99	–95	dB
@ 100 kSPS, T_{MIN} to T_{MAX}		–93			–95		dB
Signal-to-Noise and Distortion Ratio (S/(N+D))[2, 3]							
@ 83 kSPS, T_{MIN} to T_{MAX}	89	91		90	92		dB
@ 100 kSPS, +25°C	89	91		90	92		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		89			90		dB
Peak Spurious or Peak Harmonic Component		–101			–101		dB
Intermodulation Distortion (IMD)[4]							
2nd Order Products		–102			–102		dB
3rd Order Products		–98			–98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage		–0.3		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{DD}	–10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	–10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} – 1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

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NOTES

[1]V_{REF} = 10.0 V, Conversion Rate = 100 kSPS, f_{IN} = 1.0 kHz, V_{IN} = –0.05 dB, Bandwidth = 50 kHz unless otherwise indicated. All measurements referred to a 0 dB (20 V p-p) input signal. Values are post-calibration.

[2]For other input amplitudes, refer to Figure 12.

[3]For dynamic performance with different reference values see Figure 11.

[4]fa = 1008 Hz, fb = 1055 Hz. See Definition of Specifications section and Figure 16.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	–40		+85	–40		+85	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			+1	±1.5	LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)–No Missing Codes		16		16			Bits
Bipolar Zero Error[2]		±2	±4		±1	±3	LSB
Positive, Negative FS Errors[2]							
@ 83 kSPS		±2	±4		±1	±3	LSB
@ 100 kSPS, +25°C		±2	±4		±1	±3	LSB
@ 100 kSPS		±4			±4		LSB
TEMPERATURE DRIFT[3]							
Bipolar Zero		±0.5			±0.5		LSB
Postive Full Scale		±0.5			±0.5		LSB
Negative Full Scale		±0.5			±0.5		LSB
VOLTAGE REFERENCE INPUT RANGE[4] (V_{REF})	5		10	5		10	V
ANALOG INPUT[5]							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		µs
Input Capacitance During Sample		50*			50*		pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection[6]							
V_{CC} = +12 V ± 5%		±0.5			±0.5		LSB
V_{EE} = –12 V ± 5%		±0.5			±0.5		LSB
V_{DD} = +5 V ± 10%		±0.5			±0.5		LSB
Operating Current							
V_{REF} = +5 V							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	–mA
I_{DD}		3	5		3	5	mA
Power Consumption		360	480		360	480	mW
V_{REF} = +10 V							
I_{CC}		18	24		18	24	mA
I_{EE}		18	24		18	24	–mA
I_{DD}		3	5		3	5	mA
Power Consumption		450	630		450	630	mW

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NOTES
[1]V_{REF} = 10.0 V, Conversion Rate = 100 kSPS unless otherwise noted. Values are post-calibration.
[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature at nominal supplies.
[3]Values shown are based upon calibration at +25°C with no additional calibration at temperature. Values shown are the typical variation from the value at +25 °C.
[4]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 11 for dynamic performance with other reference voltage values.
[5]See "APPLICATIONS" section for recommended input buffer circuit.
[6]Typical deviation of bipolar zero, –full scale or +full scale from min to max rating.
*For explanation of input characteristics, see "ANALOG INPUT" section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	Symbol	Min	Typ	Max	Units
Conversion Period[2, 3]	t_C	10		1000	µs
CLK Period[4]	t_{CLK}	480			ns
Calibration Time	t_{CT}			85532	t_{CLK}
Sampling Time	t_S	2			µs
Last CLK to SAMPLE Delay[5]	t_{LCS}	2.1			µs
SAMPLE Low	t_{SL}	100			ns
SAMPLE to Busy Delay	t_{SS}		30	75	ns
1st CLK Delay	t_{FCD}	50			ns
CLK Low[6]	t_{CL}	50			ns
CLK High[6]	t_{CH}	50			ns
CLK to BUSY Delay	t_{CB}		180	300	ns
CLK to SDATA Valid	t_{CD}	50	100	175	ns
CLK to SCLK High	t_{CSH}	100	180	300	ns
SCLK Low	t_{SCL}	50	80		ns
SDATA to SCLK High	t_{DSH}	50	80		ns
CAL High Time	t_{CALH}	50			ns
CAL to BUSY Delay	t_{CALB}		15	50	ns

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The maximum conversion period is specified to account for the droop of the internal sample/hold function. Operation at slower rates may degrade performance.
[3]$t_C = t_{FCD} + 16 \times t_{CLK} + t_{LCS}$.
[4]580 ns is recommended for optimal accuracy over temperature (not necessary during calibration cycle).
[5]If SAMPLE goes high before the 17th CLK pulse, the device will start sampling approximately 100 ns after the rising edge of the 17th CLK pulse.
[6]$t_{CH} + t_{CL} = t_{CLK}$ and must be greater than 480 ns.

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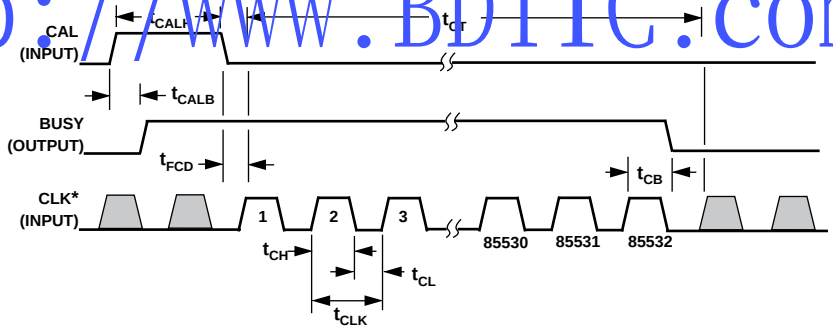

*SHADED PORTIONS OF INPUT SIGNALS ARE OPTIONAL. FOR BEST PERFORMANCE, WE RECOMMEND THAT THESE SIGNALS BE HELD LOW EXCEPT WHEN EXPLICITY SHOWN HIGH.

Figure 1. Calibration Timing

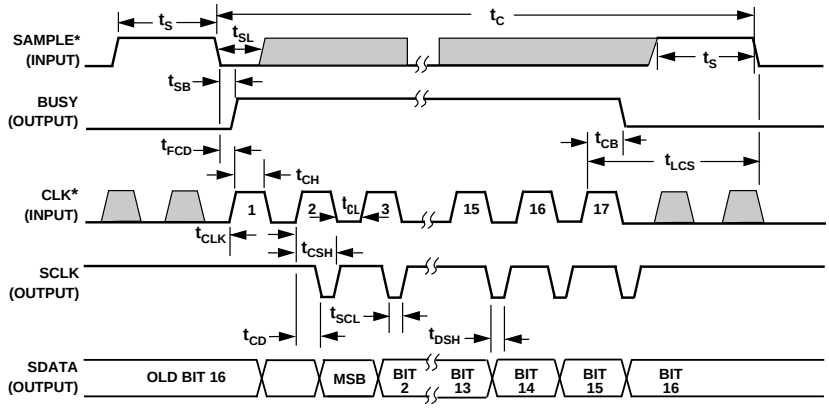

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Figure 2. General Conversion Timing

ORDERING GUIDE

Model	Temperature Range	S/(N+D)	Max INL	Package Description	Package Option*
AD677JN	0°C to +70°C	89 dB	Typ Only	Plastic 16-Pin DIP	N-16
AD677KN	0°C to +70°C	90 dB	±1.5 LSB	Plastic 16-Pin DIP	N-16
AD677JD	0°C to +70°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677KD	0°C to +70°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16
AD677JR	0°C to +70°C	89 dB	Typ Only	Plastic 28-Lead SOIC	R-28
AD677KR	0°C to +70°C	90 dB	±1.5 LSB	Plastic 28-Lead SOIC	R-28
AD677AD	–40°C to +85°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677BD	–40°C to +85°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16

*D = Ceramic DIP; N = Plastic DIP; R = Small Outline IC (SOIC).

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . –0.3 V to +26.4 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
Vcc to AGND . . . . . –0.3 V to +18 V
VEE to AGND . . . . . –18 V to +0.3 V
AGND to DGND . . . . . +0.3 V
Digiul Inputs to DGND . . . . . 0 to +5.5 V
Analog Inputs, V_{REF} to AGND
. . . . . (V_{CC} +0.3 V) to (V_{EE} –0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . –65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD677 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

DIP Pin	SOIC Pin	Type	Name	Description
1	1	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the suite of the internal sample-hold amplifier and the falling edge initiates conversion. During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on SDATA.
2	2	CLK	DI	Master Clock Input. The AD677 requires 17 clock pulses to execute a conversion. CLK is also used to derive SCLK.
3	3	SDATA	DO	Serial Output Data Controlled by SCLK.
4	6, 7	DGND	P	Digital Ground.
5	8	V_{CC}	P	+12 V Analog Supply Voltage.
8	12	AGND	P	Analog Ground.
.9	15	AGND SENSE	AI	Analog Ground Sense.
10	16	V_{IN}	AI	Analog Input Voltage.
11	17	V_{REF}	AI	External Voltage Reference Input.
12	21	V_{EE}	P	–12 V Analog Supply Voltage.
13	22, 23	V_{DD}	P	+5 V Logic Supply Voltage.
14	26	SCLK	DO	Clock Output for Data Read, derived from CLK.
15	27	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress.
16	28	CAL	DI	Calibration Control Pin.
6, 7	4, 5, 9, 10, 11, 13, 14, 18, 19, 20, 24, 25	NC	–	No Connection. No connections should be made to these pins.

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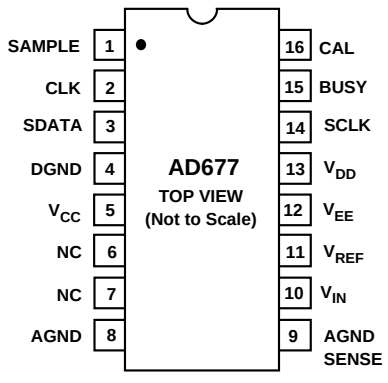
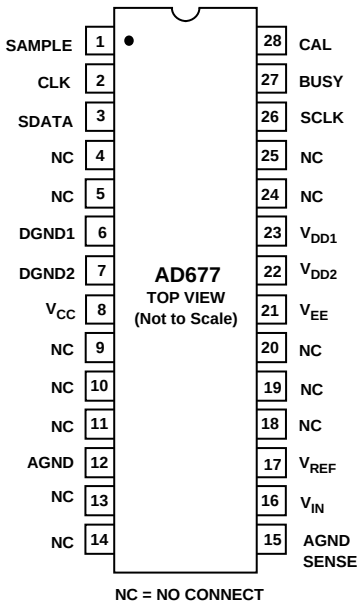
Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power



DIP Pinout



SOIC Pinout

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist frequency" of a converter is that input frequency which is one half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

+/– FULL-SCALE ERROR
The last + transition (from 011 . . . 10 to 011 . . . 11) should occur for an analog voltage 1.5 LSB below the nominal full scale (4.99977 volts for a ±5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

BIPOLAR ZERO ERROR
Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

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DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line bisecting the center of each code drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1.5 LSB beyond the most positive code transition. Integral nonlinearity is the worst-case deviation of a code center average from the straight line.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb), and the third order terms are (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY
Aperture delay is the time required after SAMPLE pin is taken LOW for the internal sample-hold of the AD677 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperture jitter is the variation in the aperture delay from sample to sample.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the overall transfer function of the ADC, resulting in zero error and full-scale error changes. Power supply rejection is the maximum change in either the bipolar zero error or full-scale error value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance. This is displayed in Figure 15.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

NOISE/DC CODE UNCERTAINTY
Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of unavoidable circuit noise within the wideband circuits in the ADC, there is a range of output codes which may occur for a given input voltage. If you apply a dc signal to the ADC and record a large number of conversions, the result will be a distribution of codes. If you fit a Gaussian probability distribution to the histogram, the standard deviation is approximately equivalent to the rms input noise of the ADC.

FUNCTIONAL DESCRIPTION

The AD677 is a multipurpose 16-bit analog-to-digital converter and includes circuitry which performs an input sample/hold function, ground sense, and autocalibration. These functions are segmented onto two monolithic chips—an analog signal processor and a digital controller. Both chips are contained within the AD677 package.

The AD677 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, this device uses a capacitor-array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the sample/hold function is included without the need for additional external circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit within the AD677. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments and is described in detail below.

The microcontroller controls all of the various functions within the AD677. These include the actual successive approximation algorithm, the autocalibration routine, the sample/hold operation, and the internal output data latch.

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AUTO CALIBRATION

The AD677 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then transferred to a capacitor of equal size (composed of the sum of the remaining lower weight bits). The voltage that results represents the amount of capacitor mismatch. A calibration digital-to-analog converter (DAC) adds an appropriate value of error correction voltage to cancel this mismatch. This correction factor is also stored in RAM. This process is repeated for each of the eight remaining capacitors representing the top nine bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results accordingly.

As shown in Figure 1, when CAL is taken HIGH the AD677 internal circuitry is reset, the BUSY pin is driven HIGH, and the ADC prepares for calibration. This is an asynchronous hardware reset and will interrupt any conversion or calibration currently in progress. Actual calibration begins when CAL is taken LOW and completes in 85,532 clock cycles, indicated by BUSY going LOW. During calibration, it is preferable for SAMPLE to be held LOW. If SAMPLE is HIGH, diagnostic data will appear on SDATA. This data is of no value to the user.

In most applications, it is sufficient to calibrate the AD677 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first. If calibration is not performed, the AD677 may come up in an unknown state, or performance could degrade to as low as 10 bits.

CONVERSION CONTROL

The AD677 is controlled by two signals: SAMPLE and CLK, as shown in Figure 2. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which execute the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum sampling time of t_S. The actual sample taken is the voltage present on V_{IN} one aperture delay after the SAMPLE line is brought LOW, assuming the previous conversion has completed (signified by BUSY going LOW). Care should be taken to ensure that this negative edge is well defined and jitter free in ac applications to reduce the uncertainty (noise) in signal acquisition. With SAMPLE going LOW, the AD677 commits itself to the conversion—the input at V_{IN} is disconnected from the internal capacitor array, BUSY goes HIGH, and the SAMPLE input will be ignored until the conversion is completed (when BUSY goes LOW). SAMPLE must be held LOW for a minimum period of time t_{SL}. A period of time t_{FCD} after bringing SAMPLE LOW, the 17 CLK cycles are applied; CLK pulses that start before this period of time are ignored. BUSY goes HIGH t_{SB} after SAMPLE goes LOW, signifying that a conversion is in process, and remains HIGH until the conversion is completed. As indicated in Figure 2, the twos complement output data is presented MSB first. This data may be captured with the rising edge of SCLK or the falling edge of CLK, beginning with pulse #2. The AD677 will ignore CLK after BUSY has gone LOW and SDATA or SCLK will not change until a new sample is acquired.

CONTINUOUS CONVERSION

For maximum throughput rate, the AD677 can be operated in a continuous convert mode. This is accomplished by utilizing the fact that SAMPLE will no longer be ignored after BUSY goes LOW, so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. If SAMPLE is already HIGH during the rising edge of the 17th CLK, then an acquisition is immediately initiated approximately 100 ns after the rising edge of the 17th clock pulse.

Care must be taken to adhere to the minimum/maximum timing requirements in order to preserve conversion accuracy.

GENERAL CONVERSION GUIDELINES

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is possible to run CLK continuously, even during the sample period. However, CLK edges during the sampling period, and especially when SAMPLE goes LOW, may inject noise into the sampling process. The AD677 is tested with no CLK cycles during the sampling period. The BUSY signal can be used to prevent the clock from running during acquisition, as illustrated

in Figure 3. In this circuit BUSY is used to reset the circuitry which divides the system clock down to provide the AD677 CLK. This serves to interrupt the clock until after the input signal has been acquired, which has occurred when BUSY goes HIGH. When the conversion is completed and BUSY goes LOW, the circuit in Figure 3 truncates the 17th CLK pulse width which is tolerable because only its rising edge is critical.

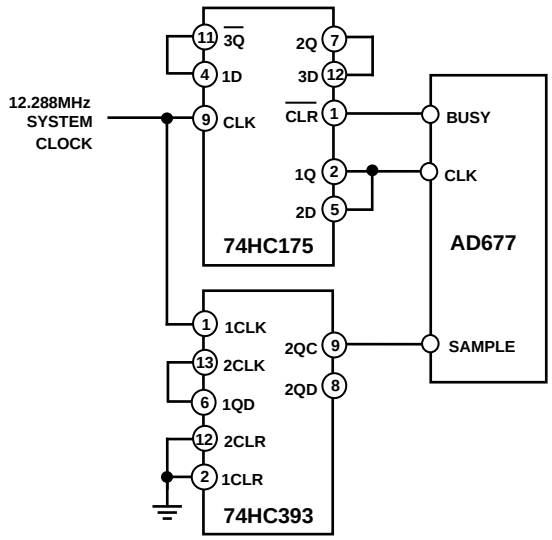

Figure 3.

Figure 3 also illustrates the use of a counter (74HC393) to derive the AD677 SAMPLE command from the system clock when a continuous convert mode is desirable. Pin 9 (2QC) provides a 96 kHz sample rate for the AD677 when used with a 12.288 MHz system clock. Alternately, Pin 8 (2QD) could be used for a 48 kHz rate.

If a continuous clock is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN} which occurs at the falling edge of SAMPLE (see t_{FCD} specification). The duty cycle of CLK may vary, but both the HIGH (t_{CH}) and LOW (t_{CL}) phases must conform to those shown in the timing specifications. The internal comparator makes its decisions on the rising edge of CLK. To avoid a negative edge transition disturbing the comparator's settling, t_{CL} should be at least half the value of t_{CLK}. It is not recommended that the SAMPLE pin change state toward the end of a CLK cycle, in order to avoid transitions disturbing the internal comparator's settling.

During a conversion, internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason there is a maximum conversion time t_C (1000 µs). From the time SAMPLE goes HIGH to the completion of the 17th CLK pulse, no more than 1000 µs should elapse for specified performance. However, there is no restriction to the maximum time between individual conversions.

Output coding for the AD677 is twos complement as shown in Table I. The AD677 is designed to limit output coding in the event of out-of-range input.

Table I. Serial Output Coding Format (Twos Complement)

V_{IN}	Output Code
<Full Scale	011 . . . 11
Full Scale	011 . . . 11
Full Scale – 1 LSB	011 . . . 10
Midscale + 1 LSB	000 . . . 01
Midscale	000 . . . 00
Midscle – 1 LSB	111 . . . 11
–Full Scale + 1 LSB	100 . . . 01
–Full Scale	100 . . . 00
<–Full Scale	100 . . . 00

POWER SUPPLIES AND DECOUPLING

The AD677 has three power supply input pins. V_{CC} and V_{EE} provide the supply voltages to operate the analog portions of the AD677 including the capacitor DAC, input buffers and comparator. V_{DD} provides the supply voltage which operates the digital portions of the AD677 including the data output buffers and the autocalibration controller.

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, and in general will increase with frequency. In other words, high frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. If these spikes exceed the ±5% tolerance of the ±12 V supplies or the ±10% limits of the +5 V supply, ADC performance will degrade. Additionally, spikes at frequencies higher than 100 kHz will also degrade performance. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD677 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. For bypassing to be effective, certain guidelines should be followed. Decoupling capacitors, typically 0.1 µF, should be placed as closely as possible to each power supply pin of the AD677. It is essential that these capacitors be placed physically close to the IC to minimize the inductance of the PCB trace between the capacitor and the supply pin. The logic supply (V_{DD}) should be decoupled to digital common and the analog supplies (V_{CC} and V_{EE}) to analog common. The reference input is also considered as a power supply pin in this regard and the same decoupling procedures apply. These points are displayed in Figure 4.

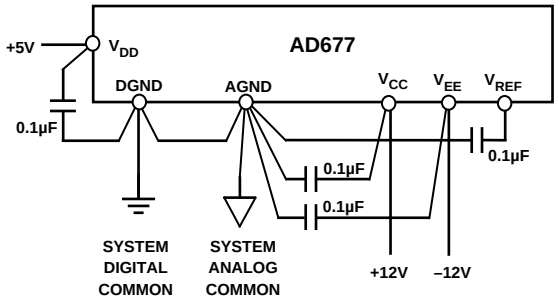

Figure 4. Grounding and Decoupling the AD677

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Additionally, it is beneficial to have large capacitors (>47 µF) located at the point where the power connects to the PCB with 10 µF capacitors located in the vicinity of the ADC to further reduce low frequency ripple. In systems that will be subjected to particularly harsh environmental noise, additional decoupling may be necessary. RC-filtering on each power supply combined with dedicated voltage regulation can substantially decrease power supply ripple effects (this is further detailed in Figure 7).

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at the AD677 to minimize interference between analog and digital circuitry. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD677 will isolate it from large switching ground currents. For these reasons the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

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GROUNDING

The AD677 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device, and should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However no more than 100 mV is recommended between the AGND and the AGND SENSE pins for specified performance.

Using AGND SENSE to remotely sense the ground potential of the signal source can be useful if the signal has to be carried some distance to the A/D converter. Since all IC ground currents have to return to the power supply and no ground leads are free from resistance and inductance, there are always some voltage differences from one ground point in a system to another.

Over distance this voltage difference can easily amount to several LSBs (in a 10 V input span, 16-bit system each LSB is about 0.15 mV). This would directly corrupt the A/D input signal if the A/D measures its input with respect to power ground (AGND) as shown in Figure 5a. To solve this problem the AD677 offers an AGND SENSE pin. Figure 5b shows how the AGND SENSE can be used to eliminate the problem in Figure 5a. Figure 5b also shows how the signal wires should be

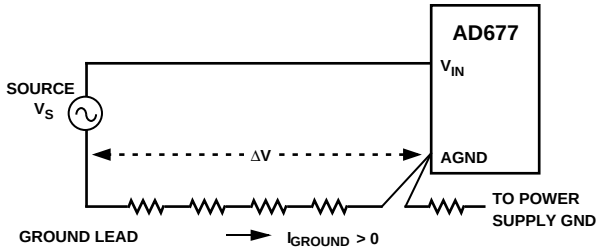

Figure 5a. Input to the A/D is Corrupted by IR Drop in Ground Leads: $V_{IN} = V_S + \Delta V$.

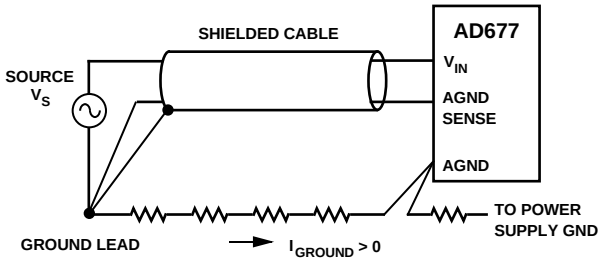

Figure 5b. AGND SENSE Eliminates the Problem in Figure 5a.

shielded in a noisy environment to avoid capacitive coupling. If inductive (magnetic) coupling is expected to be dominant such as where motors are present, twisted-pair wires should be used instead.

The digital ground pin is the reference point for all of the digital signals that operate the AD677. This pin should be connected to the digital common point in the system. As Figure 4 illustrated, the analog and digital grounds should be connected together at one point in the system, preferably at the AD677.

VOLTAGE REFERENCE

The AD677 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts allows an input range of ±n volts. The AD677 is specified for a voltage reference between +5 V and +10 V. A 10 V reference will typically require support circuitry operated from ±15 V supplies; a 5.0 V reference may be used with ±12 V supplies. Signal-to-noise performance is increased proportionately with input signal range (see Figure 12). In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance. Figure 11 illustrates S/(N+D) as a function of reference voltage. In contrast, dc accuracy will be optimal at lower reference voltage values (such as 5 V) due to capacitor nonlinearity at higher voltage values.

During a conversion, the switched capacitor array of the AD677 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. (See the following section "Analog Input" for a detailed discussion of the V_{REF} input characteristics.) The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In some applications, this may require that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. In choosing a voltage reference, consideration should be

made for selecting one with low noise. A capacitor connected between REF IN and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components required to be sourced by the reference.

Figures 6 and 7 represent typical design approaches.

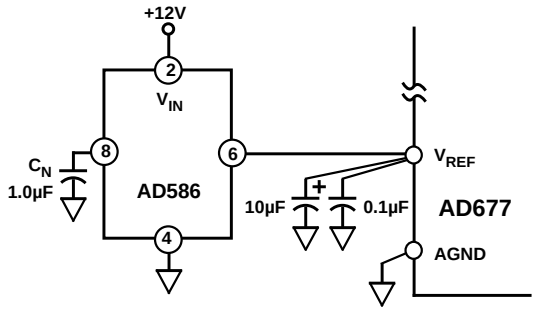

Figure 6.

Figure 6 shows a voltage reference circuit featuring the 5 V output AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586M grade exhibits less than 1.0 mV output change from its initial value at +25°C. A noise reduction capacitor, C_N, reduces the broadband noise of the AD586 output, thereby optimizing the overall performance of the AD677. It is recommended that a 10 µF to 47 µF high quality tantalum capacitor and a 0.1 µF capacitor be tied between the V_{REF} input of the AD677 and ground to minimize the impedance on the reference.

Using the AD677 with ±10 V input range (V_{REF} = 10 V) typically requires ±15 V supplies to drive op amps and the voltage reference. If ±12 V is not available in the system, regulators such as 78L12 and 79L12 can be used to provide power for the AD677. This is also the recommended approach (for any input range) when the ADC system is subjected to harsh environments such as where the power supplies are noisy and where voltage spikes are present. Figure 7 shows an example of such a system based upon the 10 V AD587 reference, which provides a 300 µV LSB. Circuitry for additional protection against power supply disturbances has been shown. A 100 µF capacitor at each regulator prevents very large voltage spikes from entering the regulators. Any power line noise which the regulators cannot eliminate will be further filtered by an RC filter (10 Ω/10 µF) having a –3 dB point at 1.6 kHz. For best results the regulators should be within a few centimeters of the AD677.

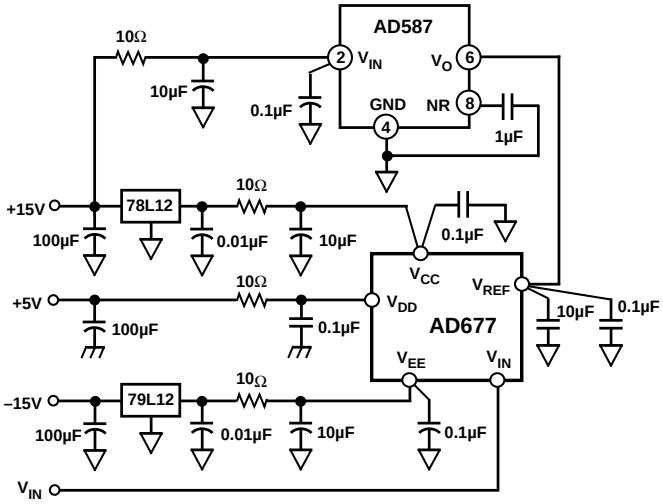

Figure 7.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD677 is $\pm V_{REF}$. For purposes of ground drop and common mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal.

The AD677 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 µA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, these characteristics require the use of an external op amp to drive the input of the AD677. Care should be taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD677. Figure 8 represents a circuit, based upon the AD845, which will provide excellent overall performance.

For applications optimized more for low distortion and low noise, the AD845 of Figure 8 may be replaced by the AD743.

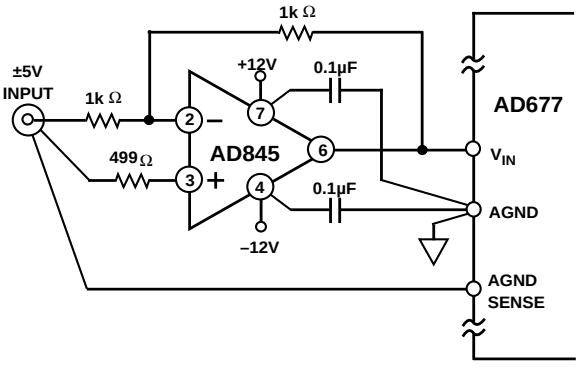

Figure 8.

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AC PERFORMANCE

AC parameters, which include S/(N+D), THD, etc., reflect the AD677's effect on the spectral content of the analog input signal. Figures 11 through 18 provide information on the AD677's ac performance under a variety of conditions.

A perfect n-bit ADC with no errors will yield a theoretical quantization noise of $q/\sqrt{12}$, where q is the weight of the LSB. This relationship leads to the well-known equation for theoretical full-scale rms sine wave signal-to-noise plus distortion level of S/(N + D) = 6.02 n + 1.76 dB, here n is the bit resolution. An actual ADC, however, will yield a measured S/(N + D) less than the theoretical value. Solving this equation for n using the measured S/(N + D) value yields the equation for effective number of bits (ENOB):

$$ENOB = \frac{\left[S/\left(N+D\right)\right]_{ACTUAL} - 1.76\ dB}{6.02}$$

As a general rule, averaging the results from several conversions reduces the effects of noise, and therefore improves such parameters as S/(N+D). AD677 performance may be optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal be sampled at a rate corresponding to at least twice its highest frequency component of interest in order to preserve the informational content. Oversampling is a conversion technique in which the sampling frequency is more than twice the frequency bandwidth of interest. In audio applications, the AD677 can operate at a $2 \times F_S$ oversampling rate, where F_S = 48 kHz.

In quantized systems, the informational content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency noise and signal components. Antialias, or low pass, filters are used at the input to the ADC to reduce these noise and signal components so that their aliased components do not corrupt the baseband spectrum. However, wideband noise contributed by the AD677 will not be reduced by the antialias filter. The AD677 quantization noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall affect.

The AD677 quantization noise effects can be reduced by oversampling—sampling at a rate higher than that defined by the Nyquist theorem. This spreads the noise energy over a bandwidth wider than the frequency band of interest. By judicious selection of a digital decimation filter, noise frequencies outside the bandwidth of interest may be eliminated.

The process of analog to digital conversion inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by S/(N + D) = (6.02n + 1.76 + 10 log $F_S/2F_A$) dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and Fa is the signal bandwidth of interest. For audio bandwidth applications, the AD677 is capable of operating at a 2 × oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are lessened. In summary, system performance is optimized by running the AD677 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DC PERFORMANCE

The self-calibration scheme used in the AD677 compensates for bit weight errors that may exist in the capacitor array. This mismatch in capacitor values is adjusted (using the calibration coefficients) during conversion and provides for excellent dc linearity performance. Figure 19 illustrates the DNL plot of a typical AD677 at +25°C. A histogram test is a statistical method for deriving an A/D converter's differential nonlinearity. A ramp input is sampled by the ADC and a large number of conversions are taken and stored. Theoretically the codes would all be the same size and, therefore, have an equal number of occurrences. A code with an average number of occurrences would have a DNL of "0". A code with more or less than average will have a DNL of greater than or less than zero LSB. A DNL of –1 LSB indicates missing code (zero occurrences).

Figure 20 illustrates the code width distribution of the DNL plots of Figure 19.

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DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of unavoidable circuit noise within the wideband circuits in the ADC, there is range of output codes which may occur for a given input voltage. If you apply a dc signal to the AD677 and record 10,000 conversions, the result will be a distribution of codes as shown in Figure 9 (using a 10 V reference). If you fit a Gaussian probability distribution to the histogram, the standard deviation is approximately equivalent to the rms input noise of ADC.

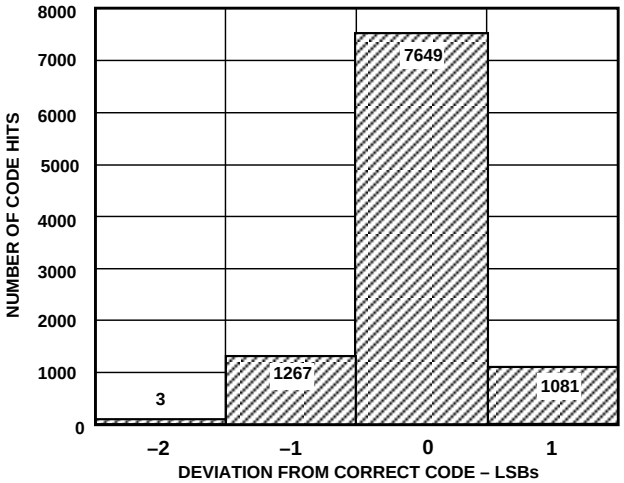

Figure 9. Distribution of Codes from 10,000 Conversions Relative to the Correct Code

The standard deviation of this distribution is approximately 0.5 LSBs. If less uncertainty is desired, averaging multiple conversions will narrow this distribution by the inverse of the square root of the number of samples; i.e., the average of 4 conversions would have a standard deviation of 0.25 LSBs.

DSP INTERFACE

Figure 10 illustrates the use of the Analog Devices ADSP-2101 digital signal processor with the AD677. The ADSP-2101 FO (flag out) pin of Serial Port 1 (SPORT 1) is connected to the SAMPLE line and is used to control acquisition of data. The ADSP-2101 timer is used to provide precise timing of the FO pin.

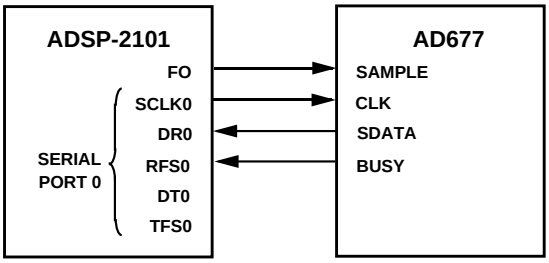

Figure 10. ADSP-2101 Interface

The SCLK pin of the ADSP-2101 SPORT0 provides the CLK input for the AD677. The clock should be programmed to be approximately 2 MHz to comply with AD677 specifications. To minimize digital feedthrough, the clock should be disabled (by setting Bit 14 in SPORT0 control register to 0) during data acquisition. Since the clock floats when disabled, a pulldown resistor of 12 kΩ–15 kΩ should be connected to SCLK to ensure it will be LOW at the falling edge of SAMPLE. To maximize the conversion rate, the serial clock should be enabled immediately after SAMPLE is brought LOW (hold mode).

The AD677 BUSY signal is connected to RF0 to notify SPORT0 when a new data word is coming. SPORT0 should be configured in normal, external, noninverting framing mode and can be programmed to generate an interrupt after the last data bit is received. To maximize the conversion rate, SAMPLE should be brought HIGH immediately after the last data bit is received.

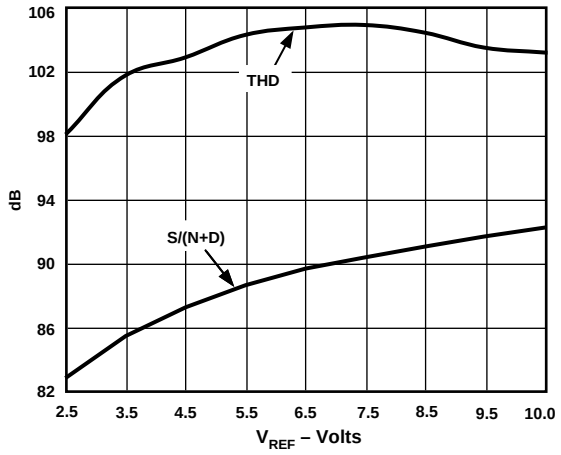

Figure 11. S/(N+D) and THD vs. V_{REF}, f_S = 100 kHz (Calibration is not guaranteed below +5 V_{REF})

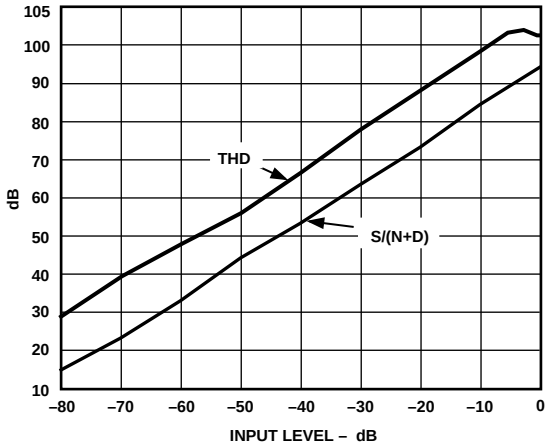

Figure 12. S/(N+D) and THD vs. Input Amplitude, f_S = 100 kHz

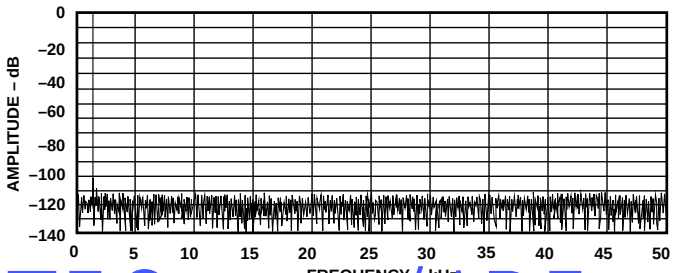

Figure 13. 4096 Point FFT at 100 kSPS, f_{IN} = 1 kHz, V_{REF} = 5 V

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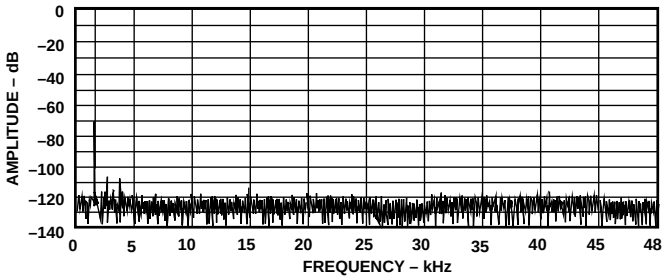

Figure 14. 4096 Point FFT at 100 kSPS, f_{IN} = 1 kHz, V_{REF} = 10 V

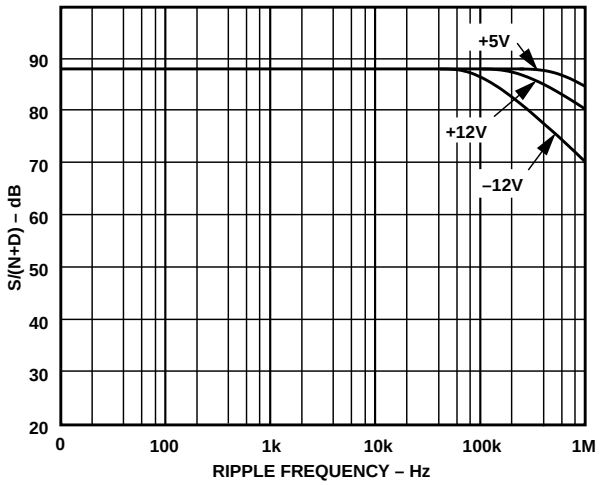

Figure 15. AC Power Supply Rejection (f_{IN} = 1.06 kHz) f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.13 V p-p

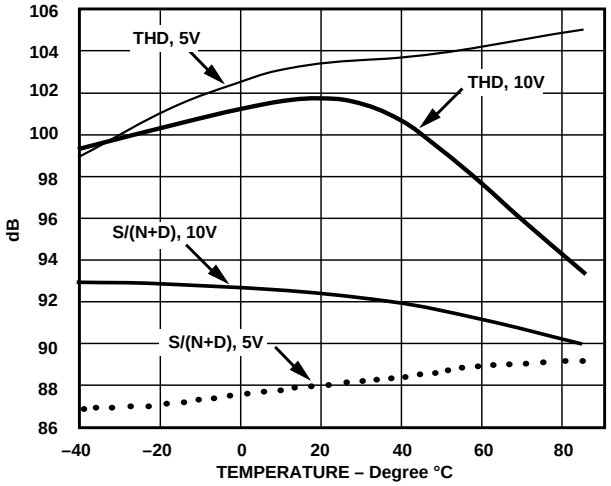

Figure 18. AC Performance Using Minimum Clock Period vs. Temperature (t_{CLK} = 480 ns), 5 V and 10 V Reference

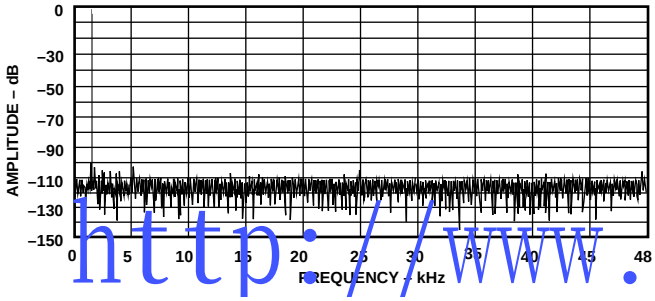

Figure 16. IMD Plot for f_{IN} = 1008 Hz (fa), 1055 Hz (fb) at 96 kSPS

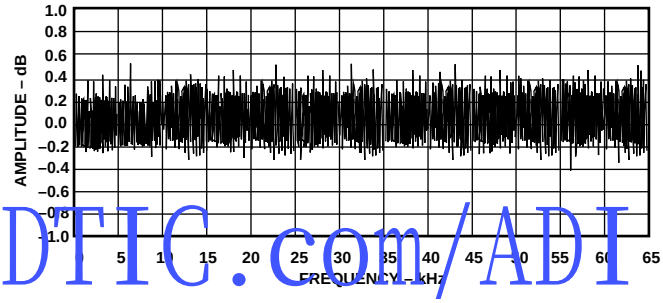

Figure 19. DNL Plot at V_{REF} = 10 V, T_A = +25°C, f_S = 100 kSPS

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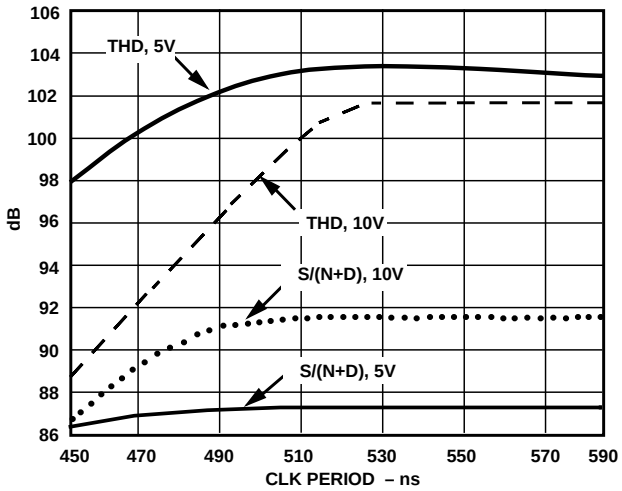


Figure 17. AC Performance vs. Clock Period, T_A = +85°C (5 V and 10 V Reference)

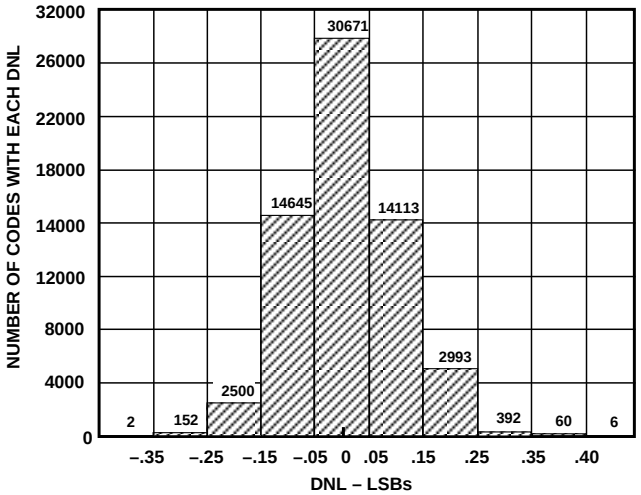
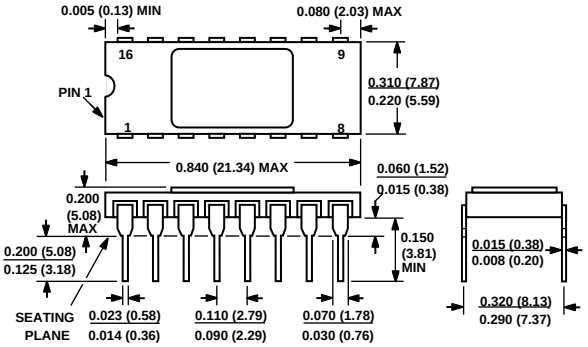


Figure 20. DNL Error Distribution (Taken from Figure 19)

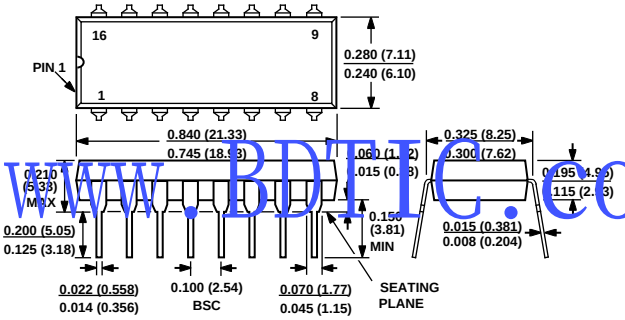
OUTLINE DIMENSIONS

Dimensions shown in inchcs and (mm)

D-16
16-Lead Side Brazed Ceramic DIP Package



N-16
16-Lead Plastic DIP



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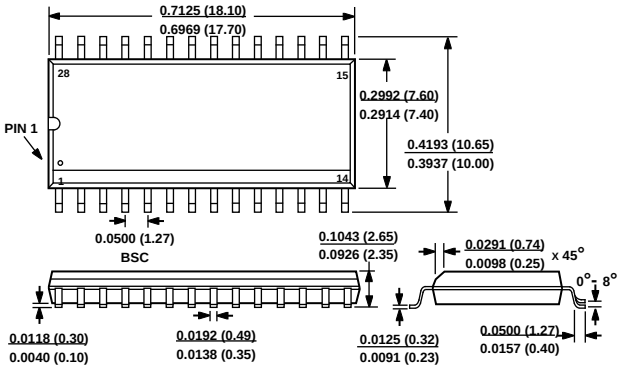
R-28
28-Lead Wide Body SOIC (SOIC-28)



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